tag for the packet with reference to the guide and the destination address; and (b) routing the packet through the network using the routing tag.

In accordance with another method aspect of the present invention, a method for self-routing a packet through a $2^n \times 2^n$ switch, the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1b_2...b_n$, and is composed of a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$, wherein each of the switching cells is a sorting cell associated with the partial order "0 ('0-bound') $\prec$ 1 ('1-bound')", the packet being destined for a binary output address $d_1d_2...d_n$, includes: (a) generating a routing tag $d_{\gamma(1)}d_{\gamma(2)}...d_{\gamma(k)}$ for the packet with reference to the guide and the destination output address of the packet; and (b) routing the packet through the network by using $d_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.

In accordance with a broad system aspect of the present invention, a $2^n \times 2^n$ self-routing switch having an array of 2^n external input ports and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1b_2...b_n$ for switching a packet, the packet being either a real data packet destined for an n-bit binary destination address, or being an idle packet having no pre-determined destination output address, includes: (a) a switch fabric with external input ports, the switch fabric having a plurality of switching cells interconnected into a k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$, where γ is a mapping from the set $\{1, 2, \ldots, k\}$ to the set $\{1, 2, \ldots, n\}$; (b) a routing tag circuit, coupled to the external input ports,

for generating a routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ for each of the real data packets with reference to the guide of the bit-permuting network and the destination output address of the packet; and (c) a routing control circuit, coupled to the switching cells, for routing the real data packet through the switch by using $1d_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to emit the packet.—

Please replace lines 1-3 on page 13 as follows: --

FIG. 21B depicts a (1 2 3) permutation on an 8×8 exchange;

FIG. 21C depicts a (3 1) permutation on an 8×8 exchange;

FIG. 21D depicts a combined (1 4)(2 3) permutation on an 8×8 exchange;--.

Page 175, replace line 9 as follows: --from the tag, by a simple dedicated 1×1 switching circuitry which is appended to every--.

Page 177, replace line 13 as follows: --10 ('0-bound') $\prec$ 00 ('idle') $\prec$ 11 ('1-bound').--.

Page 179, replace line 18 as follows: --of a bit-permuting network. The routing tag for the particular $2^n \times 2^n$ networks studied in the prior--.

Page 180, replace line 1 as follows: --art is the destination address $d_1d_2\ldots d_n$ of a packet plus possibly an activity bit up front. By--.

Please replace all of page 227, namely, the "Abstract of the Disclosure", with the following:

--<u>ABSTRACT OF THE DISCLOSURE</u>